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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/889,460	12/17/2001	Jean-Jacques Yon	2541-000008	4022

7590 01/25/2005

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Bloomfield Hills, MI 48303

EXAMINER	
JOHNSTON, PHILLIP A	

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/889,460	YON ET AL.	
	Examiner	Art Unit	
	Phillip A Johnston	2881	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This Office Action is submitted in response to amendment dated 11-09-2004. Claims 17-32 are pending.

Claims Rejection – 35 U.S.C. 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,300,915, to Higashi.

Higashi (915) clearly discloses an array of microbridge detectors each having two levels, upper 11 and lower 12, where upper level 11 of adjacent detectors (pixels) are supported by a bridging layer 20 of Silicon Nitride, and at least two sloping support legs. Lower level 12 contains integrated circuit 15. See Column 1, line 38-65; Column 2, line 27-47; Column 3, line 33-51; and Figures 1,3 and 5, below.

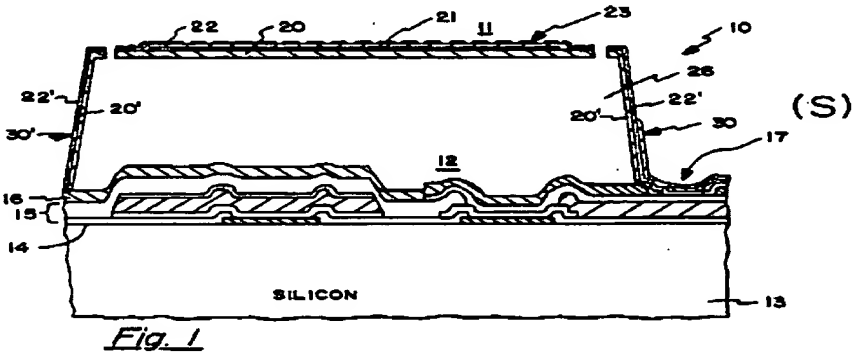

Fig. 1

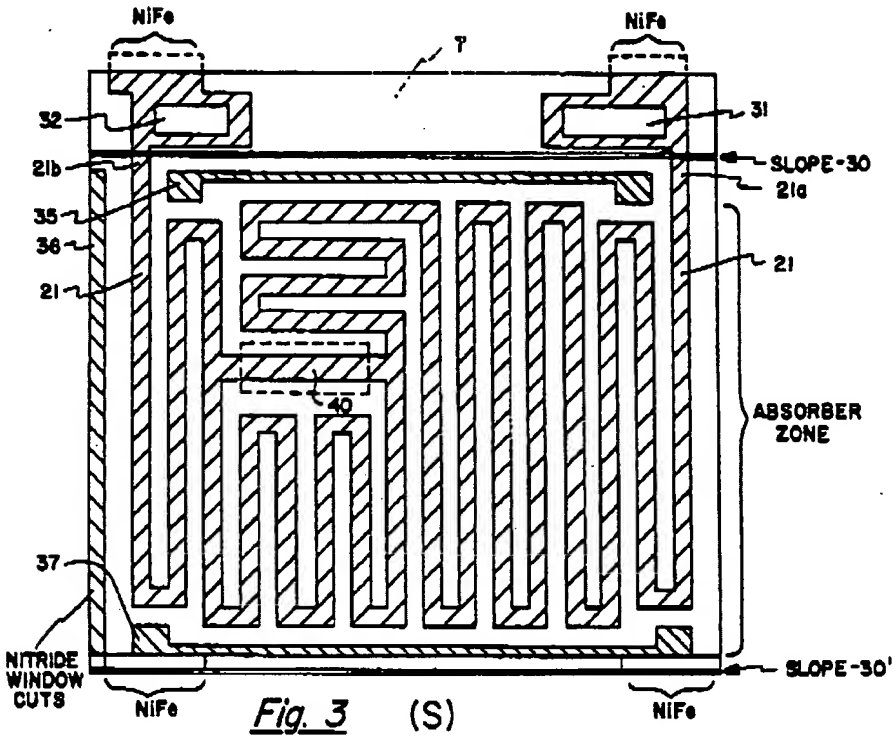
NiFe
NiFe
T
32
31
21b
SLOPE-30
21a
35
36
21
21
40
ABSORBER ZONE
37
NITRIDE WINDOW CUTS
NiFe
NiFe
SLOPE-30'

Fig. 3 (S)

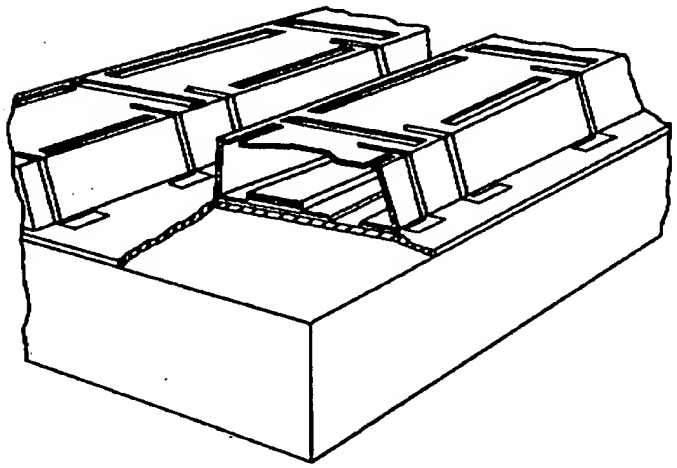

Fig. 5 (S)

Claims Rejection – 35 U.S.C. 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 22-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,300,915, to Higashi, in view of Hornbeck (663), U.S. Patent No. 5,021,663.

Regarding claim 22, Higashi (915) discloses a process for fabricating a microbridge array that includes;

(a) Forming the cavity 26 by first filling it with a previously deposited layer of easily dissolvable glass or other dissolvable material until the layers 20, 20' and 22, 22' are deposited. Subsequently in the process the glass was dissolved out to leave the cavity, as recited in claim 22. See Column 2, line 1-11;

(b) The surface 14 of the silicon substrate 13 has fabricated thereon several components of an integrated circuit 15 including diodes, x and y bus lines, connections, and contact pads at the ends of the x and y bus lines, the fabrication following conventional silicon IC technology. The integrated circuit 15 is coated with a protective layer of silicon nitride 16. A top plan view of the lower level is shown in FIG. 2 and comprises a y-diode metal (via) and a x-diode metal (via), chrome-gold-chrome

x and y bus lines, a y-side bus conductor contact 18, an x-side contact 19, and the silicon nitride protective layer, as recited in claims 22,23,30 and 31. Se Column 1, line 43-68.

(c) Fabrication steps for the upper level includes, following the deposition of the silicon nitride layer 16 in fabricating the lower level 12 and the cuts of the x-side contact area 19, the y-side bus conductor contact area 18, the cuts of the x-pads and y-pads, the lower level of electronic components and conductors is complete. The construction of the upper level 11 is then ready to commence. A layer of phos-glass or other easily soluble material approximately 3 microns thick is deposited and delineated along x-direction strips and the strip slopes 30 and 30' are thoroughly rounded to eliminate slope coverage problems. In the delineation the glass is cut to less than one micron on the strip 17. The remaining glass is cut to open the strip, and the external glass areas including the x-pad and y-pad. The upper plane silicon nitride base layer 20 is then deposited, the nickel-iron resistance layer 21 is deposited, delineated, and connected to the lower plan contacts 18 and 19, and covered with silicon nitride passivation layer 22. The trim site 40 (FIG. 3) is cut, x-pads and y-pads are opened, the absorber coating 23 is deposited and delineated, and finally the side slots 35, 36 and 37 are ion milled allowing the phos-glass to be dissolved from beneath the detector plane, as recited in claims 22,23,30 and 31. See Column 3, line 3-28.

It is implied herein that the use of conventional silicon IC technology to fabricate the microbridge detectors in accordance with Higashi (915) is equivalent to specific processing steps, as recited in claims 22, and 27-30.

Higashi (915) as applied above fails to teach the use of reflector on the surface of the processing circuit (as recited in claim 22), a heat sensitive amorphous layer (as recited in claim 23), a conductive titanium nitride layer (as recited in claim 24), and an aluminum layer(as recited in claim 25) . However, Hornbeck (663) discloses in Figures 4a and 4b the use of amorphous silicon, titanium nitride and aluminum to fabricate bolometers in a process equivalent to that recited in claims 22-25. See Column 8, 32-56; and Column 13, line 22-26.

Therefore it would have been obvious to one of ordinary skill in the art that the optical coupler of Higashi (915) can be modified to use a GRIN lens in accordance with Hornbeck (663), to provide a process for fabricating high fill factor arrays, and to maximize the signal voltage amplitude (which is the responsitivity multiplied by the incident power).

Examiners Response to Arguments

6. Applicant's arguments filed 11-09-2004 have been fully considered but they are not persuasive.

Argument 1.

Applicant states that "It is respectfully submitted that Higashi fails to disclose the features and the arrangement of features as stated in independent Claim 17 and dependent Claims 18-21, which depend therefrom."

Applicant also states that, "Higashi also does not implement a specific link between two neighbouring detectors by means of additional mechanical connections (linkages) between active areas of neighboring detectors. Further, Higashi does not show such linkages separate from the mechanical support."

The applicant is respectfully directed to Higashi (915), Column 1, line 57-66, which states; Referring again to FIG. 1, the elevated detector level 11 includes a silicon nitride layer 20, a serpentine metallic resistive layer 21, such as of nickel-iron, often called permalloy, a silicon nitride layer 22 over the layers 20 and 21, and an IR absorber coating 23 over the silicon nitride layer 22. The absorber coating may also be of a nickel-iron alloy. Downwardly extending silicon nitride layers 20' and 22' deposited at the same time during the fabrication make up the four sloping support legs for the elevated detector level.

Also Column 2, line 49-56, which states; Although the description has been basically in terms of individual detector pixels, the invention is directed to an x,y array assembly of adjoining pixels forming an imaging or mosaic detector array. Each pixel assembly may cover an area about 50 microns on a side, for example. FIG. 5 and 6 as well as FIG. 3a show a section of the array. FIG. 5 shows in perspective the sensing ridges of abutting sensors in a column. This figure is partially cutaway to show the lower level and the cavity as well.

Also, Figure 5 below.

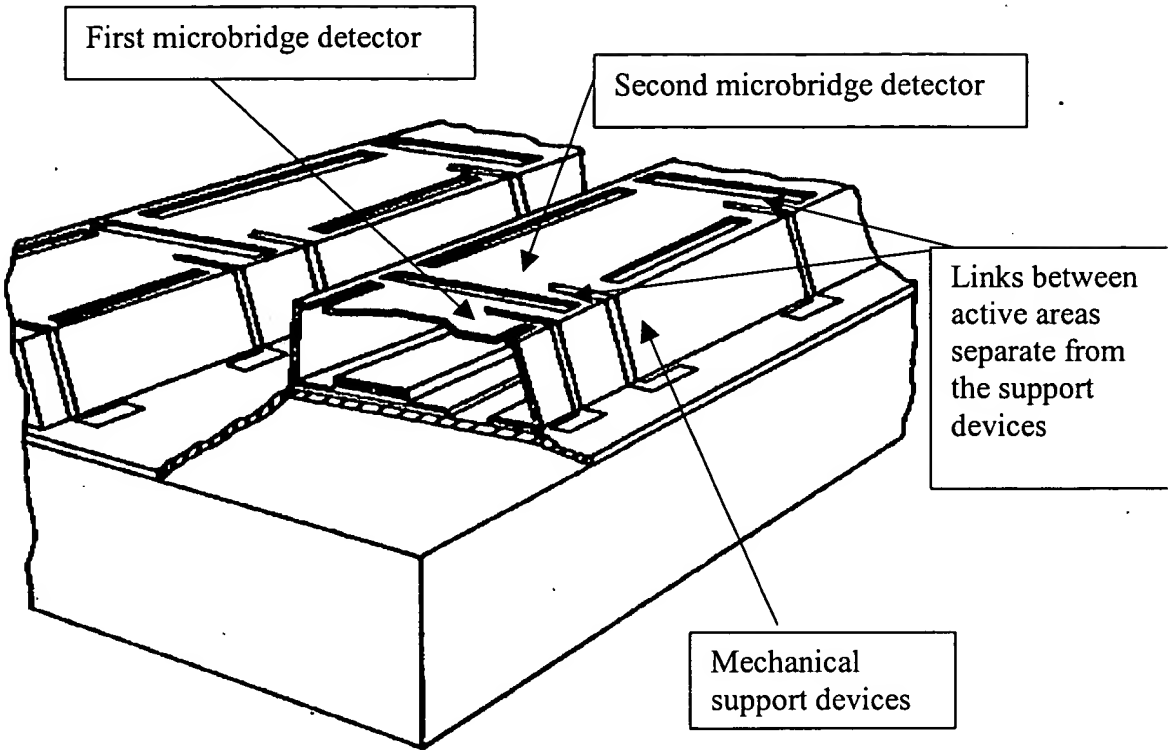

Fig. 5 (S)

The examiner has interpreted from the Higashi (915) references above, particularly Figure 5 (with highlighted notations), in light of Figure 1 that, Higashi's (915) use of layers 20,21, and 22 as the bridging layers, provide the linkage between adjacent detectors and provide mechanical connections separate from the support devices, equivalent to the structure of applicants invention, as recited in claims 17-21.

Argument 2.

Applicant states that, "Claims 22-32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Higashi in view of Hornbeck (U.S. Pat. No. 5,021,663).

Claims 22-32 are directed to a process for forming the device of Claim 17 and depend directly or indirectly on Claim 17. It is respectfully submitted that Hornbeck does not supply the deficiencies of Higashi.

The applicant is respectfully directed to Higashi (915), Column 1, line 38-48 and Column 3, line 3-27, which state;

The elevation and/or cross section view of the two-level pitless microbridge bolometer pixel 10 is shown in FIG. 1. The device 10 has two levels, an elevated microbridge detector level 11 and a lower level 12. The lower level has a flat surfaced semiconductor substrate 13, such as a single crystal silicon substrate. The surface 14 of the silicon substrate 13 has fabricated thereon several components of an integrated circuit 15 including diodes, x and y bus lines, connections, and contact pads at the ends of the x and y bus lines, the fabrication following conventional silicon IC technology. The integrated circuit 15 is coated with a protective layer of silicon nitride 16. A top plan view of the lower level is shown in FIG. 2 and comprises a y-diode metal (via) and a x-diode metal (via), chrome-gold-chrome x and y bus lines, a y-side bus conductor contact 18, an x-side contact 19, and the silicon nitride protective layer.

Further described below is a sequence of fabrication steps for the upper level. Following the deposition of the silicon nitride layer 16 in fabricating the lower level 12 and the cuts of the x-side contact area 19, the y-side bus conductor contact area 18,

the cuts of the x-pads and y-pads, the lower level of electronic components and conductors is complete. The construction of the upper level 11 is then ready to commence. A layer of phos-glass or other easily soluble material approximately 3 microns thick is deposited and delineated along x-direction strips and the strip slopes 30 and 30' are thoroughly rounded to eliminate slope coverage problems. In the delineation the glass is cut to less than one micron on the strip 17. The remaining glass is cut to open the strip, and the external glass areas including the x-pad and y-pad. The upper plane silicon nitride base layer 20 is then deposited, the nickel-iron resistance layer 21 is deposited, delineated, and connected to the lower plan contacts 18 and 19, and covered with silicon nitride passivation layer 22. The trim site 40 (FIG. 3) is cut, x-pads and y-pads are opened, the absorber coating 23 is deposited and delineated, and finally the side slots 35, 36 and 37 are ion milled allowing the phos-glass to be dissolved from beneath the detector plane.

The examiner has interpreted from the Higashi (915) references above and the Hornbeck (663) references cited previously that, the fabrication steps of Higashi (915) and Hornbeck (663), as well as the applicants are those used in conventional IC technology. For example, Higashi (915) and Hornbeck (663), utilize silicon nitride, sacrificial layers, reflective layers, conductive layers, and electrode layers to fabricate a microbridge array with conventional coating ,etching, masking and IC processing, resulting in a device structure equivalent to claim 17, which is produced in the same way with the same results as the applicants device using fabrication steps of claims 22-32.

In response to applicant's arguments that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies [i.e., The Higashi arrangement does not isolate the active detection zone (upper level) from the integrated circuit level (lower level).] are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

7. The Amendment filed on 11-09-2004 under 37 CFR 1.131 has been considered but is ineffective to overcome the Higashi (915) and Hornbeck (663) references.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications should be directed to Phillip Johnston whose telephone number is (571) 272-2475. The examiner can normally be reached on Monday-Friday from 7:30 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor John Lee can be reached at (571) 272-2477. The fax phone number for the organization where the application or proceeding is assigned is 703 872 9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PJ
January 18, 2005

JOHN R. LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800